AMENDMENTS TO THE SPECIFICATION

Amend paragraph [0051] as follows:

[0051] In particular~~concrete~~, the memory element of the present invention, which may be constructed of one first conductive type region that is the diffusion region, a second conductive type region that is the channel region, one memory function body arranged across regions of the first and second conductive types, and an electrode provided via the gate insulation film, should properly be constructed of a gate electrode formed on the gate insulation film, two memory function bodies formed on both sides of the gate electrode, two diffusion regions arranged on both sides of the memory function body oppositely to the gate electrode, and a channel region arranged under the gate electrode.

Amend paragraph [0060] as follows:

[0060] In order to improve the reliability of storage retention, the film that has the charge retention function is not always required to have a film-like shape, and a film having the charge retention function should preferably exist discretely in the insulation film. In particular~~concrete~~, it is preferred that the film having the charge retention function is distributed in a dot-like form in a material that hardly retains electric charges, or, for example, silicon oxide.

Amend paragraph [0070] as follows:

[0070] The memory element of the present invention can be formed by the ordinary semiconductor process according to a method similar to the method of forming a side wall spacer of a single layer or laminate structure on the side wall of the gate electrode. In particular~~concrete~~, there can be enumerated: a method for forming a gate electrode, thereafter forming a single layer film or a multilayer film including a film having the charge retention function (hereinafter referred to as a "charge retaining film"), a charge retaining film such as a charge retaining film/insulation film, an insulation film/charge retaining film and an insulation film/charge retaining film/insulation film and leaving these films in a side wall spacer shape by etching back under appropriate conditions; a method for forming an insulation film or a charge retaining film, leaving the films in a side wall spacer shape by etching back under appropriate conditions, further forming a charge retaining film or an insulation film and leaving the films in a side wall spacer shape by etching back under appropriate conditions; a method for coating or depositing an insulation film material in which a particulate charge retaining material is distributed on a semiconductor layer including a gate electrode, and leaving the insulation film material in a side wall spacer shape by etching back under appropriate conditions; a method for forming a gate electrode, thereafter forming the single

layer film or the multilayer film and carrying out patterning by using a mask and so on. Moreover, there can be enumerated a method for forming a charge retaining film, a charge retaining film/insulation film, an insulation film/charge retaining film, an insulation film/charge retaining film/insulation film and so on before forming the gate electrode, forming an opening in a region that becomes a channel region of these films, forming a gate electrode material film on the entire upper surface and patterning this gate electrode material film in a shape, which is larger than the opening and includes the opening and so on.

Amend paragraph [0080] as follows:

[0080] Moreover, the device is more useful when the requirements (3) and (9) are satisfied and the requirement (6) is satisfied. That is, by making the charge retaining region and the diffusion region in each memory function body overlap with each other, the write and erase operations can be executed at a very low voltage. In particular~~concrete~~, the write and erase operations can be executed at a low voltage of not higher than 5 V. This operation produces a very large effect in terms of circuit design. There is no need to make a high voltage in a chip dissimilarly to the flash memory, and therefore, the charge pump circuit, which requires an enormous occupation area, can be eliminated or reduced in scale. Particularly, when a small-scale capacity memory for adjustment is built in a logic LSI, the

occupation area of the memory section is dominated by the occupation area of the peripheral circuit for driving the memory cells than the memory cells. Therefore, it is most effective to eliminate or reduce the scale of the memory cell voltage booster circuit in order to reduce the chip size.

Amend paragraph [0109] as follows:

[0109] Moreover, it is to be noted that the drawings are schematic, and the dimensional relations between thickness and plane, ratios of thickness and size between layers and portions and so on are different from those of the actual ones. Therefore, the specific ~~concrete~~ dimensions of thickness and size should be determined in consideration of the following description. Moreover, there are, of course, included the portions whose mutual dimensional relations and ratios are different between the figures.

Amend paragraph [0169] as follows:

[0169] As clearly shown in Fig. 19, when write operation is performed in the erased state (a solid line), as shown by a broken line, not only the threshold value simply rises, but inclination of the graph dramatically falls especially in sub-threshold region. Therefore, even in the region with relatively high gate voltage (Vg), a drain current ratio of the erased state to the written state is large. For example in the point

of Vg=2.5V, the current ratio is still two digits or more. This characteristic is largely different from that in the case of a flash memory shown in Fig. 23~~29~~.

Amend paragraph [0188] as follows:

[0188] This portable telephone is made up mainly of a control circuit 811, a battery 812, an RF (Radio Frequency) circuit 813, a display section 814, an antenna 815, a signal line 816 a power line 817. A semiconductor storage device 811a of the present invention described above is incorporated into the control circuit 811. The control circuit 811 should preferably be an integrated circuit where devices of an identical structure are concurrently used as a memory circuit element and a logic circuit element. This facilitates the manufacturing of integrated circuits and allows the manufacturing cost of the portable electronic equipment to be especially reduced.